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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/772,982	02/04/2004	Baher S. Haroun	TI-27596.2	5472	
23494	7590 06/30/2006		EXAM	EXAMINER	
TEXAS INS	TRUMENTS INCORE	BONURA, TIMOTHY M			
	P O BOX 655474, M/S 3999 DALLAS, TX 75265		ART UNIT	PAPER NUMBER	
,			2114		
			DATE MAILED: 06/30/2006		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
Office Action Summany	10/772,982	HAROUN ET AL.				
Office Action Summary	Examiner	Art Unit				
	Tim Bonura	2114				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DOWN THE MAILING	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tim will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	N. nely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on <u>04 August 2004</u> .						
	, -					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) Claim(s) <u>1 and 2</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1 and 2</u> is/are rejected.						
7) Claim(s) is/are objected to.	n alaatian raguinamant					
8) Claim(s) are subject to restriction and/o	r election requirement.					
Application Papers						
9)☐ The specification is objected to by the Examine	r.					
10)⊠ The drawing(s) filed on <u>04 February 2004</u> is/are: a)⊠ accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Ex	aminer. Note the attached Office	Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892)	4) Interview Summary	(PTO-413)				
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5) Notice of Informal Patent Application (PTO-152)						
Paper No(s)/Mail Date	6) Other:					

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DETAILED ACTION

Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Mack, et al,
 U.S. Patent Number 5,689,516.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Mack, et al, U.S. Patent Number 5,689,516.
- 3. Regarding claim 1:
 - a. Regarding the limitation of "providing within said integrated circuit a test port linking circuit having a register for receiving a first portion of said serial instruction frame," Mack discloses a system with a JTAG port capable of receiving instruction frames. (Lines 10-13 of Column 2).
 - b. Regarding the limitation of "providing within said integrated circuit a test port circuit having a register for receiving a second portion of said serial instruction frame," Mack discloses a system with a JTAG port for receiving disable bit. (Lines 15-18 of Column 2).
 - c. Regarding the limitation of "transmitting the serial instruction frame to said registers of said test port linking and test port circuits," Mack discloses a system with a JTAG capable of receiving instructions on the TAP from a user. (Lines 15-18 of Column 4).

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d. Regarding the limitation of "responding to the instruction frame portion transmitted into the register of the test port linking circuit to disable further transmission of instruction frames into said test port circuit," Mack discloses a system with a disable bit that when programmed, disables the JTAG. (Lines 15-18 of Column 2 and Lines 28-32 of Column 4).

4. Regarding claim 2:

- e. Regarding the limitation of "providing within said integrated circuit a test port linking circuit having a register for receiving said serial instruction frame," Mack discloses a system with a JTAG port capable of receiving instruction frames. (Lines 10-13 of Column 2).
- f. Regarding the limitation of "providing within said integrated circuit a test port circuit," Mack discloses a system with a JTAG and a TAP port. (Lines 15-18 of Column 4).
- g. Regarding the limitation of "transmitting said serial instruction frame to said registers of said test port linking and test port circuits," Mack discloses a system with a JTAG capable of receiving instructions on the TAP from a user. (Lines 15-18 of Column 4).
- h. Regarding the limitation of "responding to the instruction frame transmitted into the register of the test port linking circuit to enable further transmission of further instruction frames into said test port circuit," Mack discloses a system wherein if the disable bit is a logic zero, test port circuit remains active to receive test commands. (Lines 15-28 of Column 4).

Conclusion

- 5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura**.
 - o The examiner can normally be reached on Mon-Fri: 8:30-5:00.
 - The examiner can be reached at: 571-272-3654.
- 6. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman**.
 - o The supervisor can be reached on 571-272-3644.
- 7. The fax phone numbers for the organization where this application or proceeding is assigned are:
 - o 703-872-9306 for all patent related correspondence by FAX.
- 8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
- 9. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100**.
- **10.** Responses should be mailed to:
 - o Commissioner of Patents and Trademarks

P.O. Box 1450

Alexandria, VA 22313-1450

tmb June 24, 2006

BRYCE P. BONZO PRIMARY EXAMINER